

# Measuring Power Digitally with Numerical Analysis

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## ABSTRACT

*In low-power systems, traditional power measurement techniques using Analog-to-Digital Converters (ADCs), amplifiers, and current sense resistors present a number of practical challenges; especially if one desires to monitor many components on a low power platform. This work introduces our novel digital method that attempts to minimize and/or eliminate the use of analog components while obtaining highly accurate measurements at fine resolutions using minimal power. Through our preliminary experiments, we have verified that our technique can be applied to accurately measure the power consumption of board and integrated circuits (IC) while eliminating measurement noise. Our on-going research seeks to refine and validate the core idea for measuring subcomponent power on board as well as within ICs.*

## 1. THE RESEARCH

Our research seeks to design, implement, and verify an all or mostly digital power measurement technology that enables measurement of subcomponent power on PC boards and within chips. The benefits of our technique include high measurement resolution, resilience to measurement noise, low instrumentation cost, low operational power, and high scalability.

## 2. THE METHOD

Our work is based on the most fundamental theory surrounding the relationship between transistor signal transition and its dynamic power consumption. Based on this theory, we assume that accurate power of a circuit can be computed given (1) signal transition count and (2) dissipated power per signal transition for every transistor in the circuit. However, manually instrumenting a circuit to collect these data is impractical. Therefore, we introduce a practical method of extracting these two aspects of a circuit through use of sparse instrumentation of digital counters, initial measurement of global power consumption, and a mathematical analysis.

In order to do this we, first, write an equation to represent the total power consumption of a circuit; the total power consumed by a circuit consisting  $n$  components, each consuming dynamic power  $p_{dynamic}$  and static power  $p_{static}$  can be written as the following:

$$P_{total} = \sum_{i=1}^n (p_{static,i} + p_{dynamic,i}) \quad (1)$$

If we assume  $p_{static}$  for every component is not changing, we may sum all of the static power to a single parameter  $P_{static}$ . Based on the above theory, we can also express  $p_{dynamic,i}$  as product of total signal transition (or signal activity rate)  $r_i$  and dissipated power per transition (or weight)  $w_i$ . Then we can rewrite the total power equation as the following:

$$P_{total} = P_{static} + \sum_{i=1}^n w_i r_i \quad (2)$$

We observe that  $w_i$  and  $P_{static}$  in the equation are constant values while  $r_i$  and  $P_{total}$  are dynamically changing during the operation of a circuit. Therefore, if we can obtain  $w_i$  and  $P_{static}$  for a given circuit, we can determine  $P_{total}$  given  $r_i$  and vice versa.

As mentioned before, instrumentation to make accurate  $r_i$  is impractical and self-defeating due to cost and its own power requirements. Therefore, we make an additional assumption and apply mathematical analysis to practically obtain these parameters.

The key assumption that we make to proceed with our method is that the total signal activity of a component is directly proportional to the signal transition counts of its peripheral data input and output. This assumption is based on the intuition that the sub-circuits of functional unit are interdependent. Although the peripheral signal activity may not be equal to the total number of transitions  $r_i$ , the weights  $w_i$  may be adjusted to compensate the difference.

Our method of deriving  $w_i$  and  $P_{static}$  requires that we collect an initial set of  $P_{total}$  while the circuit is running for use in our independent component analysis (ICA). At a fixed interval, we sample the  $P_{total}$  of the circuit while counting  $r_i$  for every component in the circuit. Assuming all components of the circuit are activated at some point, we can extract  $i+1$  linearly independent equation to solve for  $w_i$  and  $P_{static}$ .

In realistic scenarios, there are variations in power consumptions due to Process-Voltage-Temperature (PVT) variations. We believe that the process variation can be accounted for with our technique. Currently, we do not account for the dynamic variations in voltage and temperature during the operation.

In addition to PVT, there are a number of factors of the circuit that we categorize as residual noise. For this, we add a residual variable into our equation. By performing ICA over moving windows of time while minimizing the residual factor, we obtain  $w_i$  that converge. That is, these weights are calculated once for the given design and subsequent measurements are done by multiplying the weights with corresponding normalized count values.

Once converged values for  $w_i$  and  $P_{static}$  are obtained, we suggest that  $P_{total}$  of the circuit can be determined from the equation using subsequently counted values of  $r_i$  instead of using external instrumentation. Furthermore, we suggest that dynamic power consumption of each component can also be determined using  $w_i$  and  $r_i$ .

## 3. EXPERIMENTS

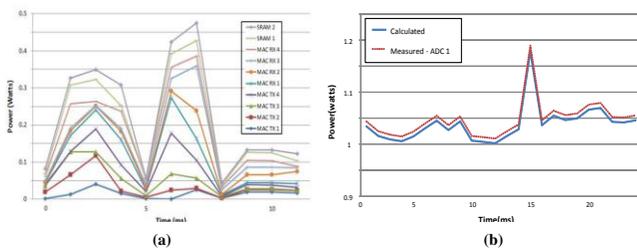
We have conducted an experiments to (1) test the feasibility of our technology and (2) measure accuracy of determining  $P_{total}$  and (3) resilience to the measurement noise.

For the first experiment, we used NetFPGA 1G for the board level power measurement due to its hardware reconfigurability and existing reference hardware designs. We used PCI-extender

board and MCC Tracer DAQ board to measure  $P_{total}$  for computing constant parameters as well as using it as the ground truth measurement.

Since most of the components of NetFPGA are connected to the main Virtex 2 Pro FPGA, we instrumented counters at every input and output pins of the FPGA. The counter values of wires connected to each component are independently summed to represent  $r_i$  for each component. All of the counter values in FPGA are also summed to represent the power consumed by FPGA itself.

For our experiment, we instrumented NetFPGA configured as an IP router with signal activity counters and sent various network traffic through the device. A subset of the collected  $r_i$  and  $P_{total}$  data (training set) is used with ICA to obtain the weights for individual components. Once the weights were found to converge, we use them on a different set of experimental data to compute power for each component as well as  $P_{total}$  then compared against the measured  $P_{total}$ .



**Figure 1: Dynamic Power for the Hardware IP Router**

In Figure 1, the various lines in part (a) indicate corresponding per-component power values on the board. The part (b) shows the graph of sum total of calculated per-component power versus the actual power measured by the data acquisition card. When we compared the total power determined through our technique with converged  $w_i$  and  $P_{static}$  against the ADC measured  $P_{total}$ , we found that the average error was 1.1 % without it ever exceeding 1.9% over several experimental runs.

In addition to this experiment, we conducted an experiment to test the noise resilience of our technique. We hypothesized that introduction of external noise that is uncorrelated to any of the internal function of the circuit would be filtered by our algorithm, causing the  $w_i$  and  $P_{static}$  to converge to the same value. Therefore, we added to our raw  $P_{total}$  data a number of different signals ranging from sinusoidal functions of different frequencies to white noise. Although the time that our algorithm took to find converged weights was dependent on the noise, they all eventually converged to the same values. Currently, we have yet to conduct more exhaustive experiments to claim noise suppression of our method. However, the initial results seem to suggest cleaner method of power measurement than traditional methods.

#### 4. WORK IN PROGRESS

Currently, we three tasks in progress: (1) accurate power measurement of a single IC, (2) sub-circuit power measurement, and (3) a custom power measurement and validation platform.

For the first task, we are using Spartan 3E starter board with a custom processing circuit instrumented with counters for obtaining  $r_i$  for functional units within the circuit. Like the board level design, we intend to show that the power of the chip can be measured by monitoring the signal activity within the circuit. Unlike the board, FPGA provides us with the flexibility

of instrumenting counters in any part of the circuit to potentially increase the accuracy of the measurements.

During our experiment for the previous task, we found that the error between the measured data and computed data was larger than expected (~5%). On the other hand, the values for  $w_i$  and  $P_{static}$  continued to converged to the same value with different set of data. Upon further investigation, we found that there may be some parts on the FPGA that was consuming power and yet was difficult to instrument with counters. Through this unexpected discovery, we devised a parallel research task to validate the sub-circuit power consumption of FPGA without having to separate the power plane. For this task, we would design two data independent circuits A and B within the FPGA. Then we will collect  $r_i$  with (1) both circuits active, (2) A active and B inactive, and (3) A inactive and B active. Then ICA will be applied to each set of data separately. If the result of this method yields the same converged weights for A between (1) and (2), B between (1) and (3), we may gain more confidence in our validity of our work.

In addition to the above tasks, we are designing a FPGA based custom PC board where each component are monitored with dedicated ADC to precisely evaluate our digital technique. We plan to show the online comparison between the measured and calculated power to capture the ground truth.

#### 5. CONCLUSION

Our work presents a novel method to measure per-component power accurately and efficiently. By comparing values of actual power measured with those obtained from our method, we conclude that the proposed method is consistent and accurate.

Due to low operational power and low instrumentation cost associated with our technology, there are several applications in low-power mobile systems. It may also be used to guide re-synthesis tasks for high performance systems where power budget is the limiting factor of their design.

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